

Form PTO-1449 U.S. Dept. of Commerce Patent & Trademark Office	Atty. Docket: 01-LJ-062	Serial No. 10/032,742
List of Documents Cited by Applicant (Use several sheets if necessary)	Applicant: Sivagnanam PARTHASARATHY et al.	
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U.S. PATENT DOCUMENTS

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FOREIGN PATENT DOCUMENTS

		Document Number	Date	Country	Class	Sub-class	Trans'n Yes/No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)

AA1	Reed Solomon Decoder: TMS320C64x Implementation; Application Report, SPRA686, December 2000.
AA2	Hasan, M.A. "An Architecture for a Universal Reed-Solomon Encoder using a Triangular Basis Multiplication Algorithm", IEEE CCECE/CCGEI, 1993, pp. 255-258.
AA3	Hasan, M.A. et al. "Efficient Architectures for Computations Over Variable Dimensional Galois Fields", IEEE Transactions on Circuits and Systems-I: Fundamental Theory and Applications, Vol. 45, No. 11, November 1998, pp. 1205-1211.
AA4	Wicker, S.B. et al. "Reed-Solomon Codes and Their Applications", IEEE Press, pp. 68-70.
AA5	Fumess, R. et al. "Multiplication Using the Triangular Basis Representation Over $GF(2^m)$ ", 1996 IEEE, pp. 788-792.
AA6	Fumess, R. et al. "Generalised Triangular Basis Multipliers for the Design of Reed-Solomon Coders", 1997 IEEE, pp. 202-211.
AA7	Paar, C. "Efficient VLSI Architectures for Bit Parallel Computation in Galois Fields", PhD Thesis, University of Essen, June 1994, Chapter 5, pp. 42-58.
AA8	Paar, C. et al. "Efficient Multiplier Architectures for Galois Fields $GF(2^m)$ ", IEEE Transactions on Computers, Vol. 47, No. 2, February 1998, pp. 162-170.
AA9	Fumess, R. et al. "GF(2 ^m) Multiplication over the Triangular Basis for Design of Reed-Solomon Codes", IEEE Proc.-Comput. Digit. Tech., Vol. 145, No. 6, November 1998, pp. 437-443.

Examiner: <u>D. H. Malzahn</u>	Date Considered: <u>3/1/05</u>
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